Basic PLC Programming 2

Chapter 6

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Bit Instructions Review

- XIC - Examine if Closed
- XIO - Examine if Open
- OTE - Output Energize
- OTL - Output Latch
- OTU- Output Unlatch

Timer instructions overview

- **Introduction**

  Timers are very important in ladder logic programming. Timers gives the precision in time. Timer on delay starts timing when instruction is true. Timers are used to track time when instruction are on or off. They could also keep track on a retentive base.

Timer instructions Parameters

The following parameters are associated with Timer instructions:

- **Preset Value (.PRE)**
  - **This specifies the value which the timer must reach before the controller sets the done bit. When the accumulated value becomes equal to or greater than the preset value, the done (DN) bit is set. You can use this bit to control an output device.**
  - **Preset and accumulated values for timers range from 0 to +32,767. If a timer preset or accumulated value is a negative number, a runtime error occurs.**

- **Accumulator Value (.ACC)**

  This is the time elapsed since the timer was last reset. When enabled, the timer updates this continually.

- **Timebase**

  The timebase determines the duration of each timebase interval. For Fixed and SLC 5/01 processors, the timebase is set at 0.01 second.

Timer Registers

Table 1.4 Timer Control Fields

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Word
EN	TT	DN							Internal Use[1]							0
Preset Value (PRE)																1
Accumulator Value (ACC)																2

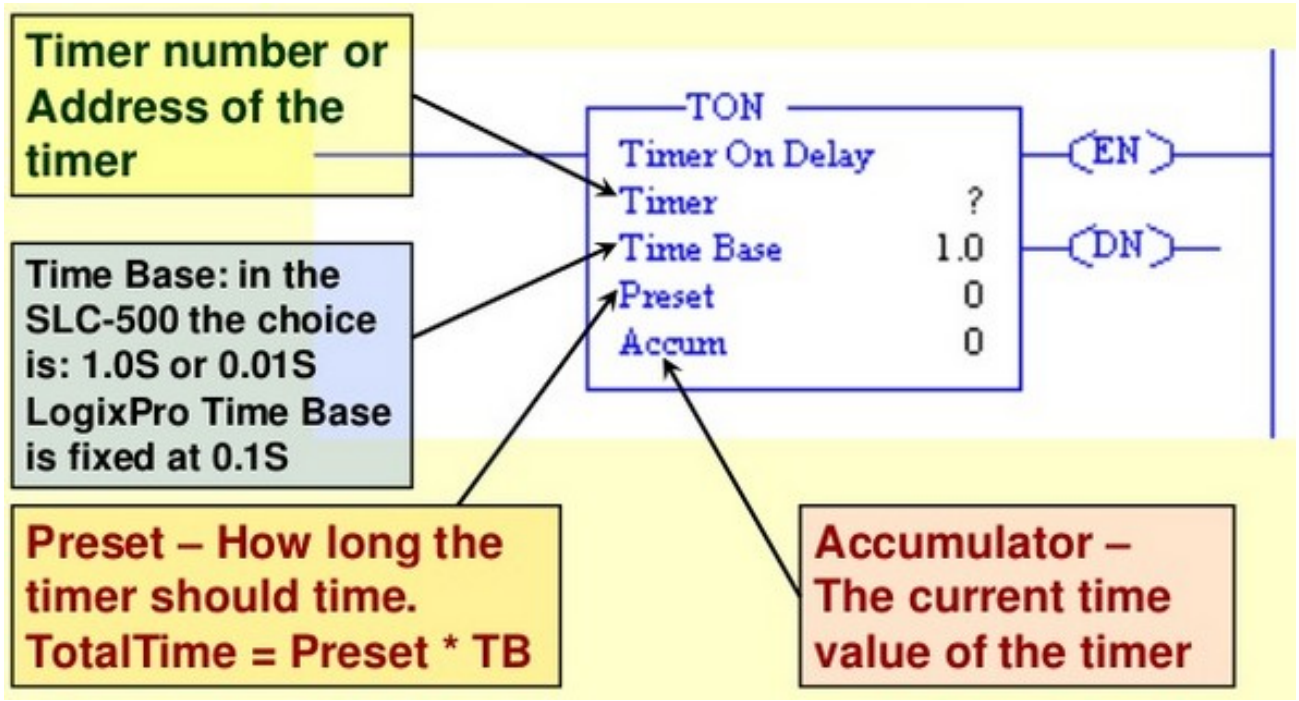
(1) Bits labeled "Internal Use" are not addressable.

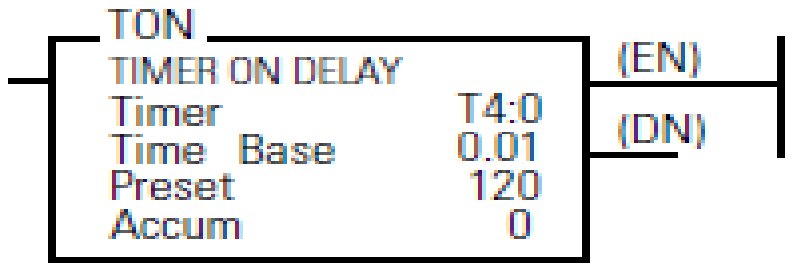
Addressable Bits	Addressable Words
EN = Enable (Bit 15)	PRE = Preset Value
TT = Timer Timing (Bit 14)	ACC = Accumulated Value
DN = Done (Bit 13)	

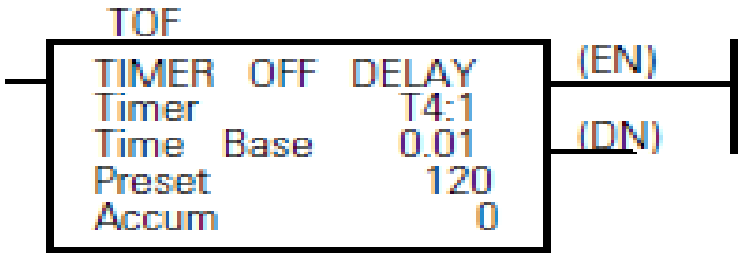
Timer Instructions

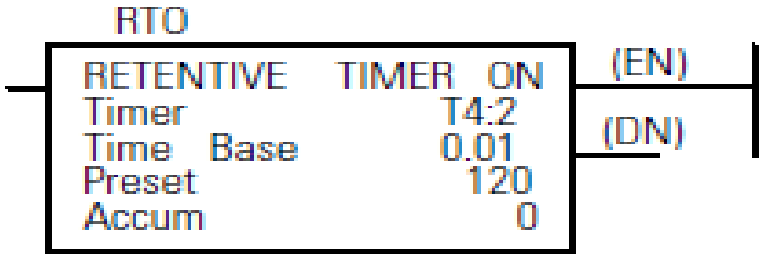
The following is a list of timer instructions in SLC 500:

- **TON - Timer On Delay**
- **TOF - Timer Off Delay**
- **RTO - Retentive Timer**



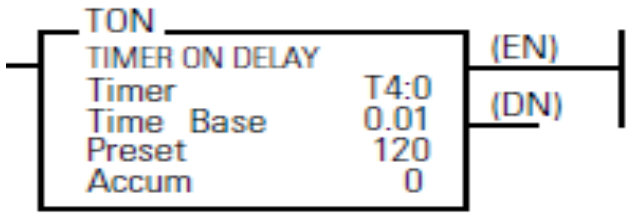


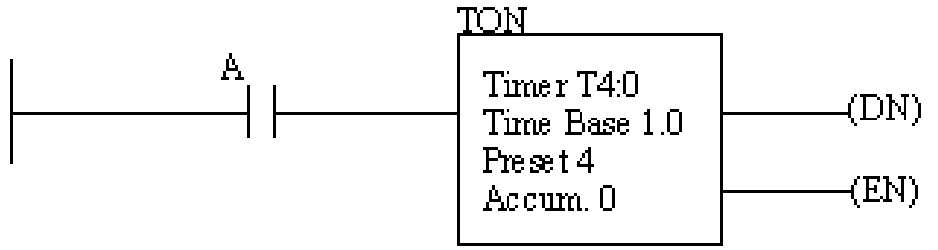




TON Timer On Delay

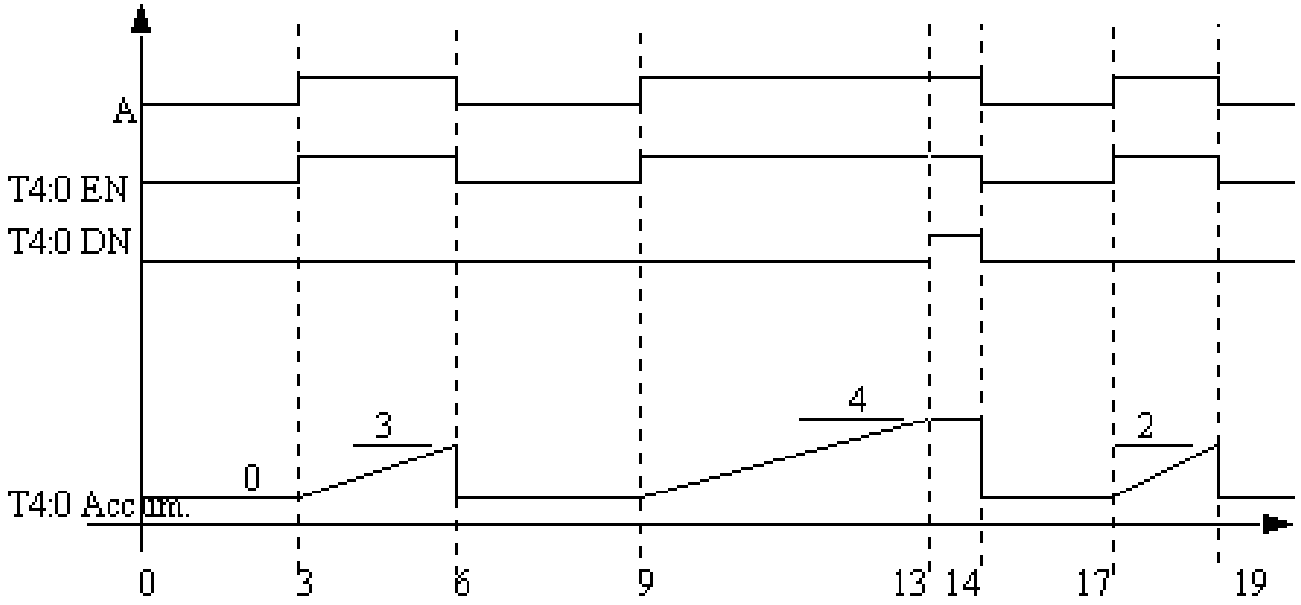
Symbol





Definition

- **Count time base intervals when the instruction is true.**
- **The Timer On Delay instruction begins to count time base intervals when rung conditions become true.**
- **As long as rung conditions remain true, the timer adjust its accumulated value (ACC) each evaluation until it reaches the preset value (PRE).**
- **The accumulated value is reset when rung conditions go false, regardless of whether the timer has timed out.**



TON Timer On Delay

Each Timer on Delay is made of a 3-word element.

- **Word 1 is the control word**

Bit 0-12: Internal Use

Bit 13: Done (DN) this bit is on when the Accumulation value >= Preset Value

Bit 14: Timer Timing (TT) this bit is on when the timer is timing

Bit 15: Enabled (EN), this bit is on when the timer is energized.

This Bit	Is Set When	And Remains Set Until One of the Following
Timer Done Bit DN (bit 13)	accumulated value is equal to or greater than the preset value	rung conditions go false
Timer Timing Bit TT (bit 14)	rung conditions are true and the accumulated value is less than the preset value	rung conditions go false or when the done bit is set
Timer Enable Bit EN (bit 15)	rung conditions are true	rung conditions go false

- **Word 2 stores the preset value. (PRE)**

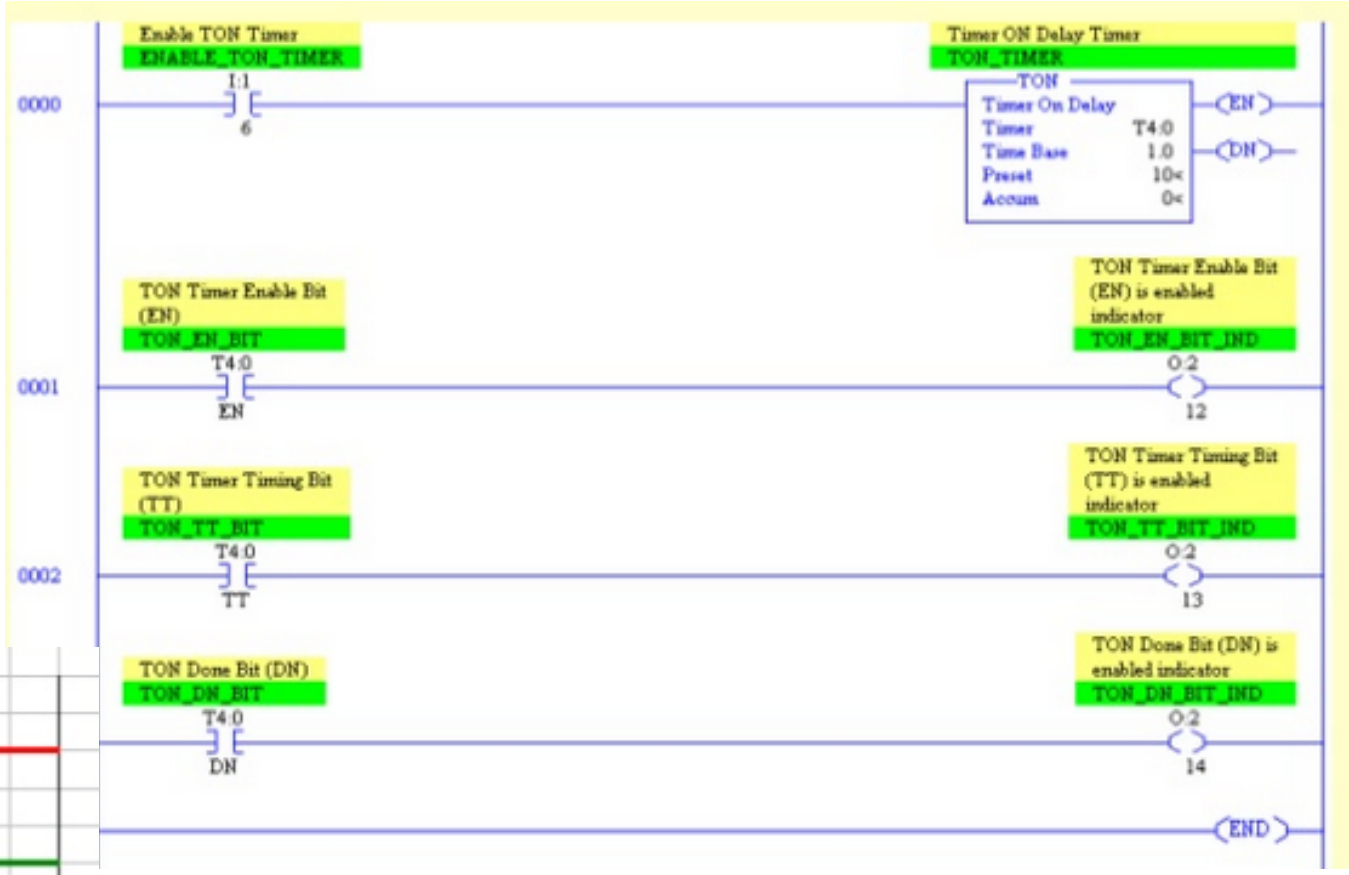
  - **The programmer specifies this value. When the accumulated time reaches the preset value the controller sets the done bit. When the accumulated value becomes equal to or greater than the preset value, the done bit is set. Usually preset value is from 0 - 32,767**
  - **If a timer-preset value is negative an error will occur.**

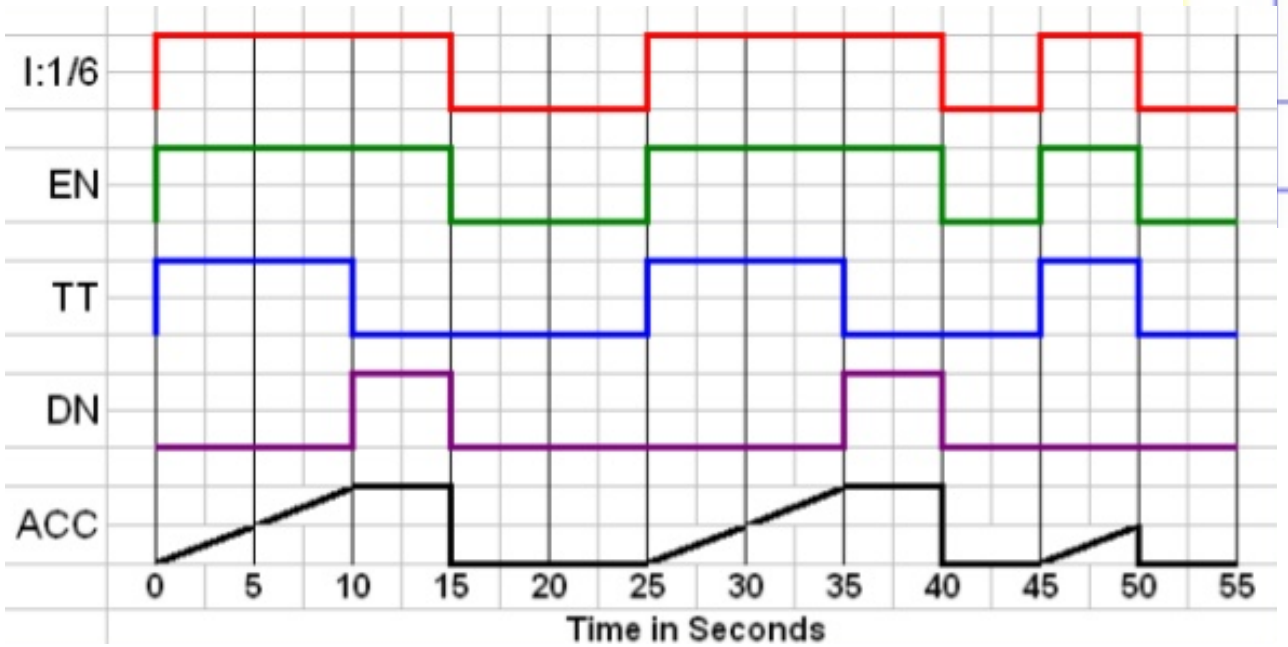
- **· Word 3 stores the accumulated value. (ACC)**

This is the time elapsed since the timer was last reset. When enabled the timer updates this continually.

Time Base: is the timing update interval.

TON Timing Diagram





Example 1

- Lets say that we have a conveyor, alarm and 1 limit switch LS-01. LS-01 is at the beginning of the conveyor. When LS-01 is ON we want a buzzer to go on for 3 seconds (Security) and then we want to start the conveyor. When LS-01 is cleared then we want to stop the conveyor.

- **Input / Output**

  Conveyor O:2.0/0

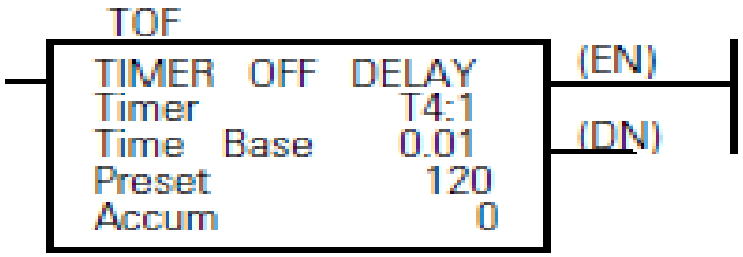
  Alarm O:2.0/1

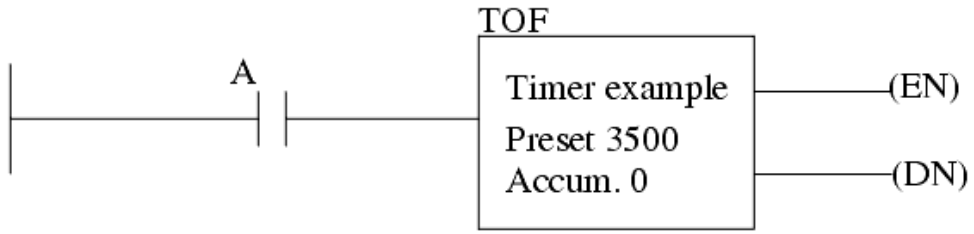
  LS-01 I:1.0/0

- **Ladder Logic Solution**

TOF Timer Off Delay

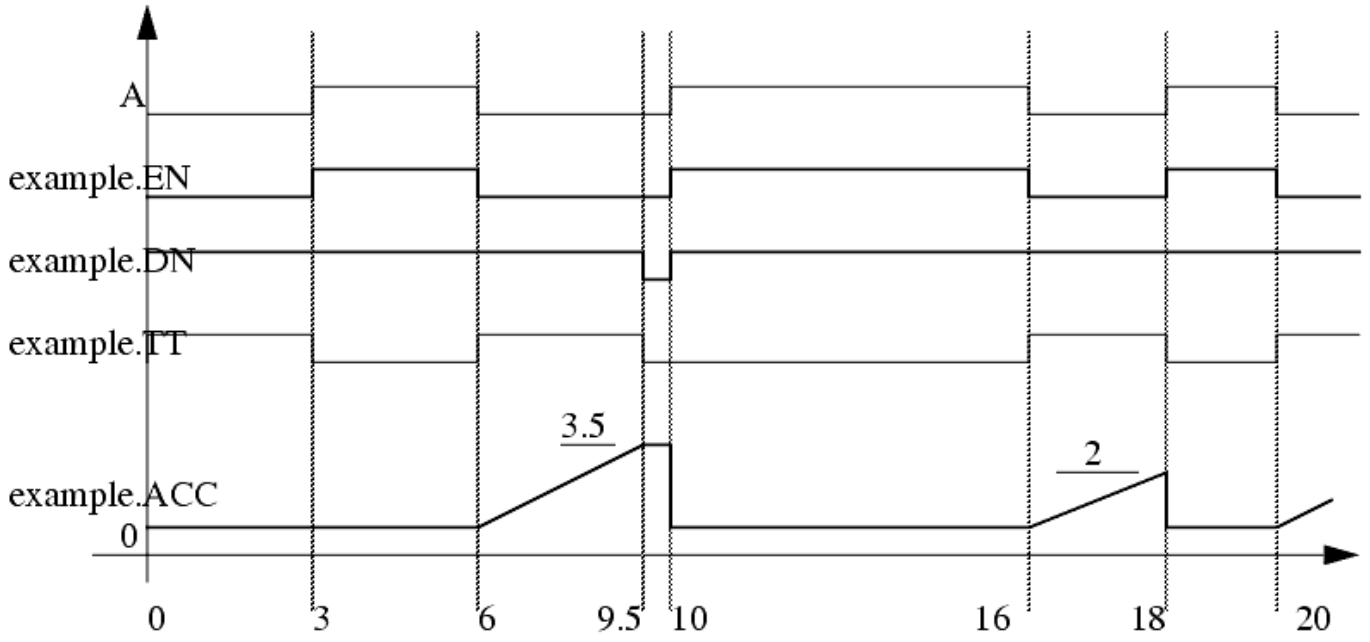
Symbol





Definition

- **Counts time base intervals when the instruction is false.**
- **The Timer Off Delay instruction begins to count time base intervals when the rung makes a true to false transition.**
- **As long as rung conditions remain false, the timer increments its accumulated value (ACC each scans until it reaches the preset value (PRE).**
- **The accumulated value is reset when rung conditions go true regardless of whether the timer has timed out.**



TOF Timer Off Delay

Each timer address is made of a 3-word element.

Word 1 is the control word

Bit 0-12: Internal Use

Bit 13: DN- Done

Bit 14: TT - Timer Timing

Bit 15: EN - Timer is enabled

Word 2 stores the preset value. (PRE)

This Bit	Is Set When	And Remains Set Until One of the Following
Timer Done Bit DN (Bit 13)	rung conditions are true	rung conditions go false and the accumulated value is greater than or equal to the preset value
Timer Timing Bit TT (Bit 14)	rung conditions are false and the accumulated value is less than the preset value	rung conditions go true or when the done bit is reset
Timer Enable Bit EN (Bit 15)	rung conditions are true	rung conditions go false

Specifies the value, which the timer must reach before the controller sets the done bit. When the accumulated value becomes equal to or greater than the preset value, the done bit is se.

Preset value is from 0 - 32,767

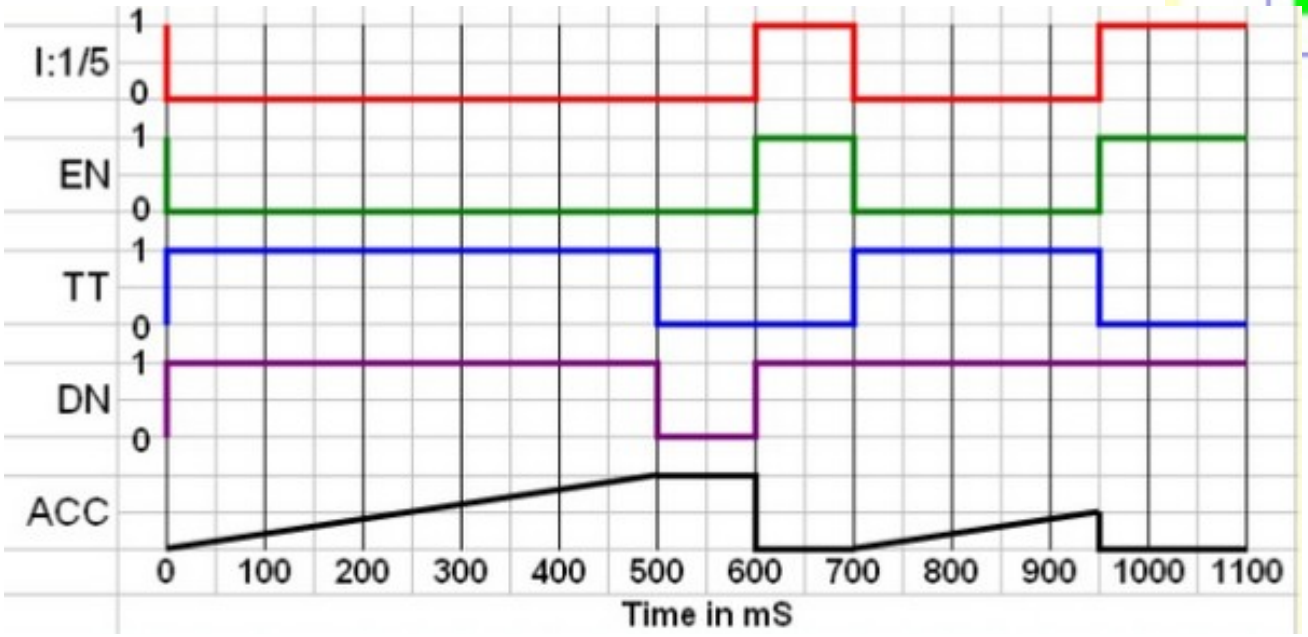
If a timer-preset value is negative an error will occur.

Word 3 stores the accumulated value. (ACC)

This is the time elapsed since the timer was last reset. When enabled the timer updates this continually.

Time Base: is the timing update interval.

TOF Timing Diagram

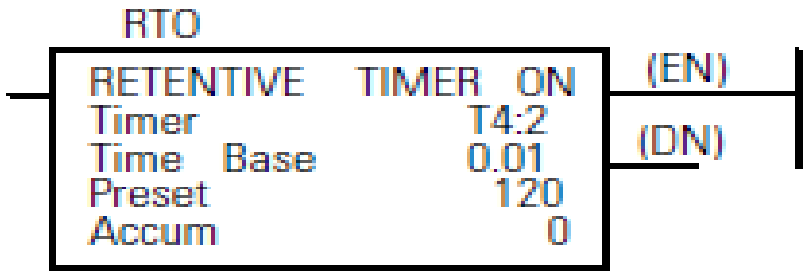


Example 2

- Let's say we have in the field an emergency stop. Once the E-Stop is pressed we want the buzzer to go on for 5 seconds.
- **Input / Output**
  - E-Stop Push Button I:1.0/0
  - Buzzer O:2.0/0
- **Ladder Logic Solution(use TOF Timer)**

RTO Retentive On-delay Timer

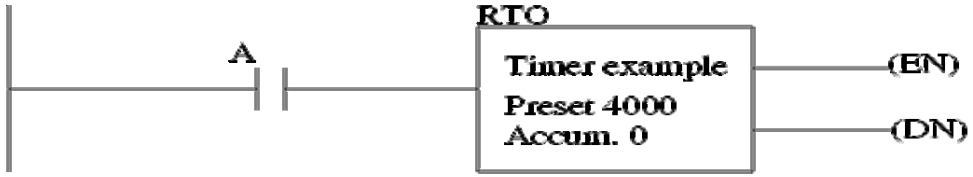
Symbol

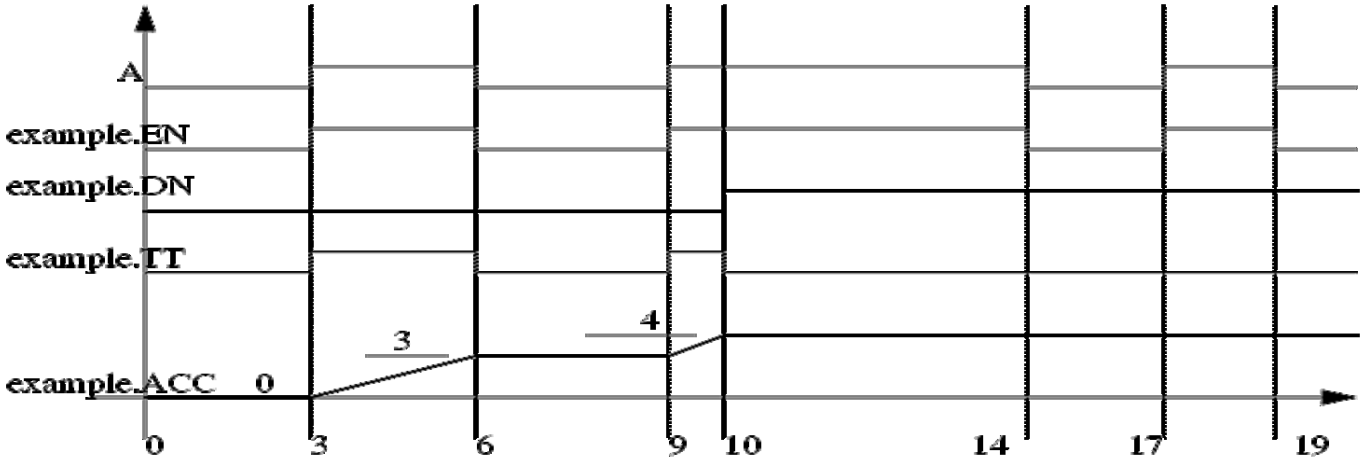


Definition

- **Counts time base intervals when the instruction is true and retains the accumulated value when the instruction goes false or when power cycle occurs.**
- **The Retentive Timer instruction is a retentive instruction that begins to count time base intervals when rung conditions become true.**
- **The Retentive Timer instruction retains its accumulated value when any of the following occurs:**
  - **Rung conditions become false.**
  - **Changing Processor mode from REM run /Test / program mode.**
  - **The processor loses power (provided that battery back up is still maintained).**
  - **A fault occurs.**

Note : To reset the accumulated value in RTO, you must use a reset instruction (RES) with the same address.





RTO Retentive On-delay Timer

Each Retentive Timer is made of a 3-word element.

Word 1 is the control word

Bit 0-12: Internal Use

Bit 13: DN- Done

Bit 14: TT - Timer Timing

Bit 15: EN - Timer is enabled

This Bit	Is Set When	And Remains Set Until One of the Following
Timer Done Bit DN (Bit 13)	accumulated value is equal to or greater than the preset value	the appropriate RES instruction is enabled
Timer Timing Bit TT (Bit 14)	rung conditions are true and the accumulated value is less than the preset value	Rung conditions go false or when the done bit is set
Timer Enable Bit EN (Bit 15)	rung conditions are true	rung conditions go false or if the timer is reset with the RES instruction

Word 2 stores the preset value. (PRE)

Specifies the value, which the timer must reach before the controller sets the done bit. When the accumulated value becomes equal to or greater than the preset value, the done bit is set.

Preset value is from 0 - 32,767

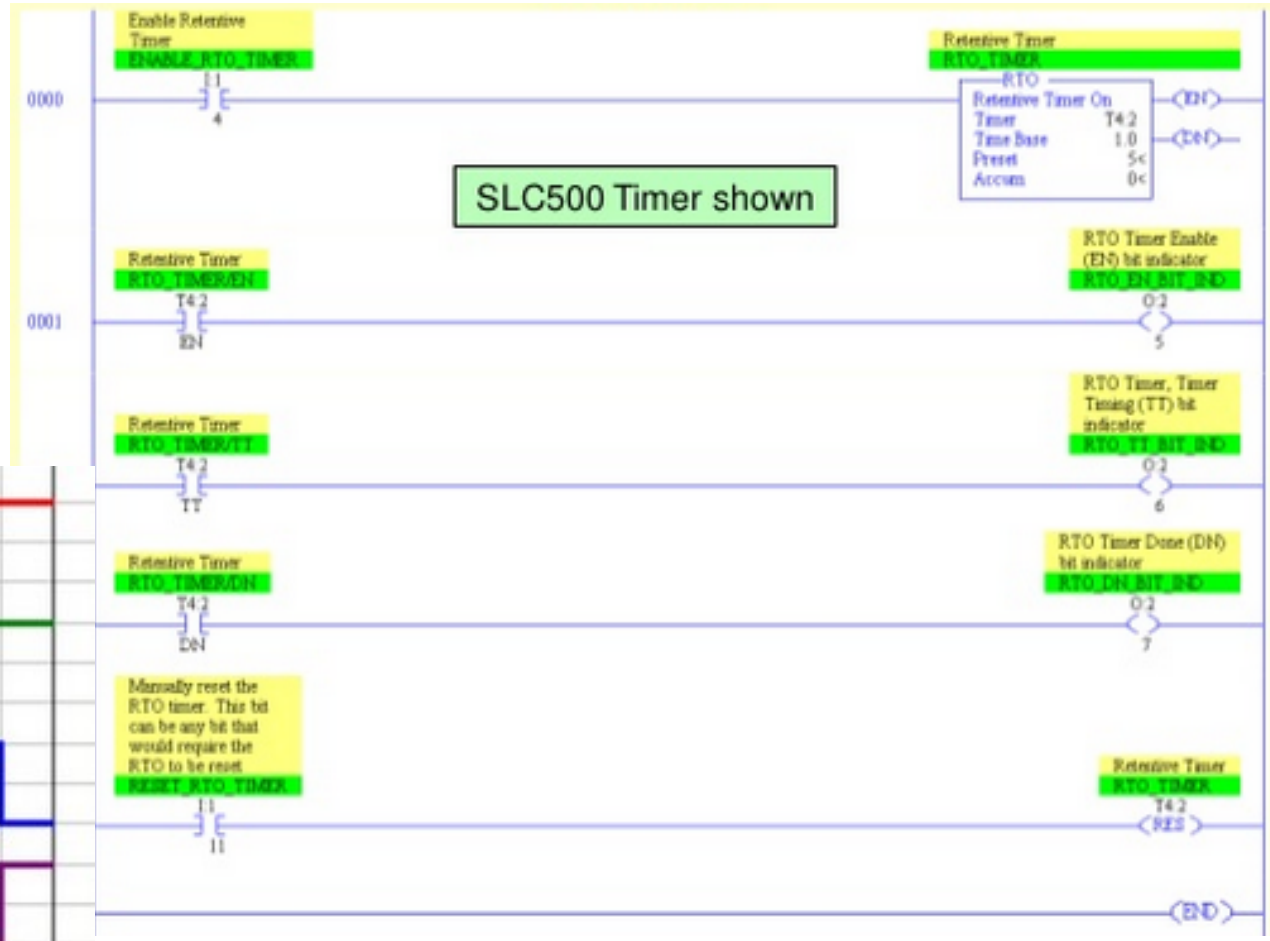
If a timer-preset value is negative an error will occur.

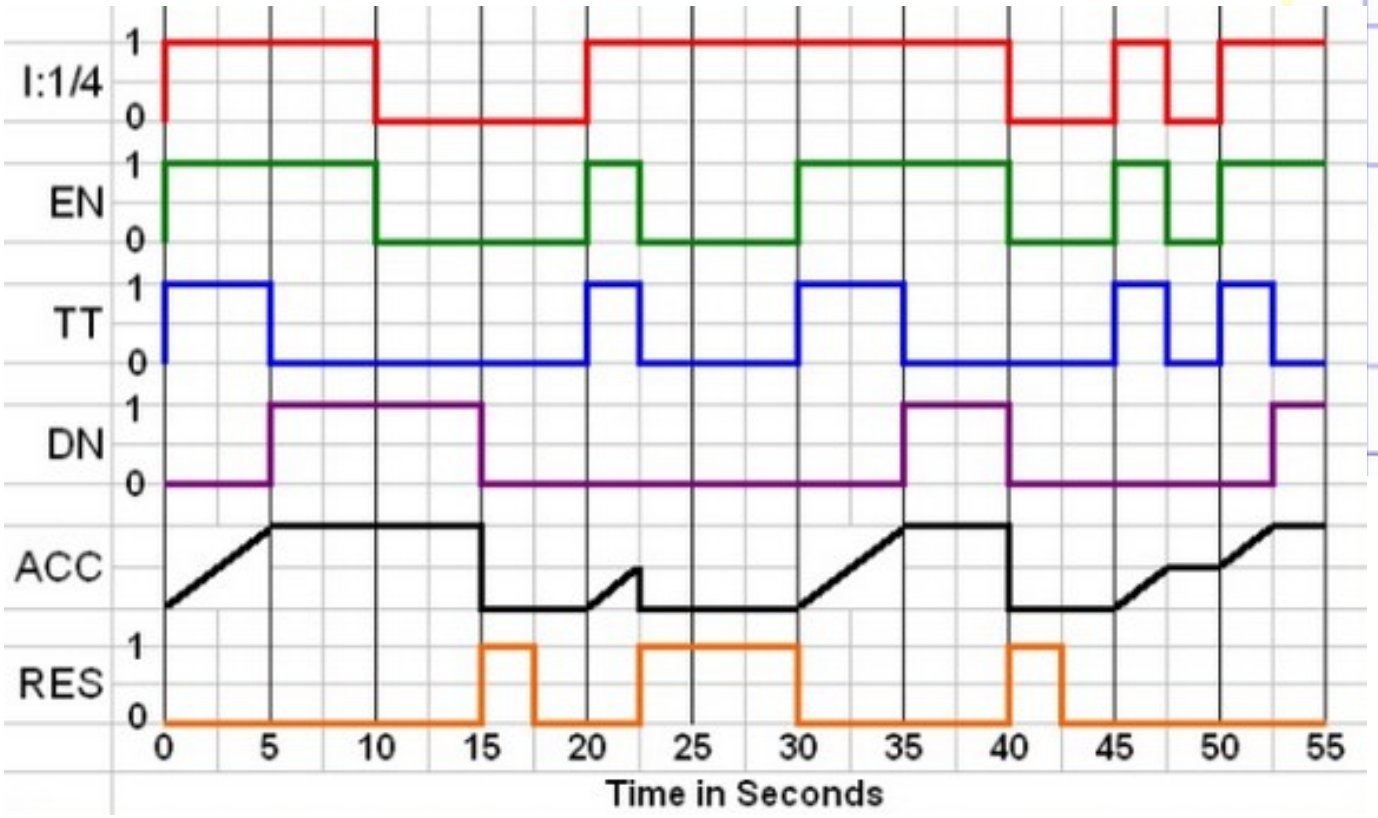
Word 3 stores the accumulated value. (ACC)

This is the time elapsed since the timer was last reset. When enabled the timer updates this continually.

Time Base: is the timing update interval.

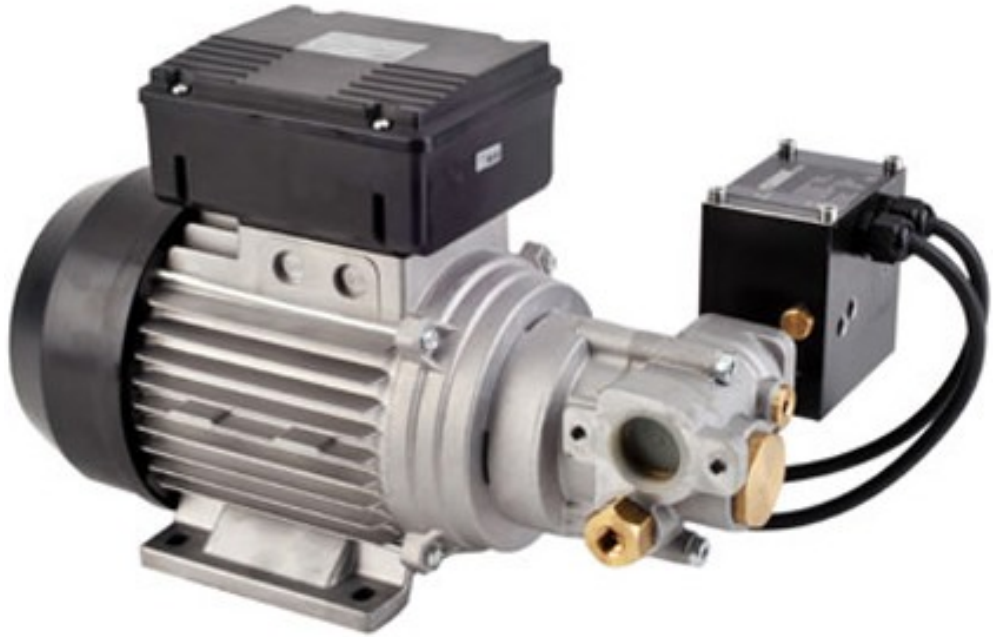
RTO Timing Diagram





Example 3

- Let's say we to have a timer on a motor that times the time the motor was on. What we want to do is to run the lubrication pump every 10 minutes the main motor has run, for 5 seconds.
- **Input / Output**
  - Selector I:1.0/0
  - Motor O:2.0/0
  - Lube Pump O:2:0/1
- **Ladder Logic Solution**



TIMERS

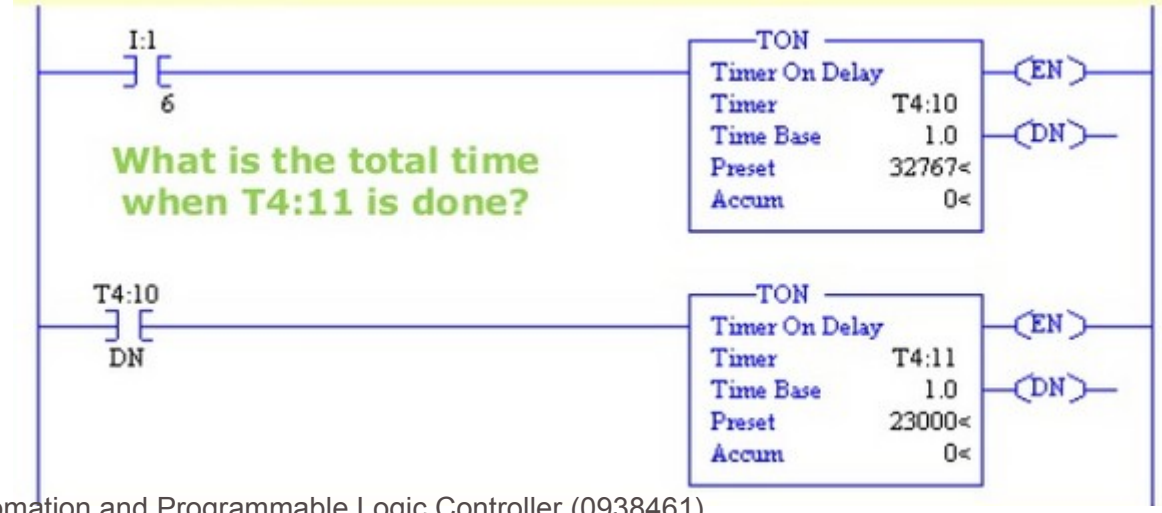
- **RESET INSTRUCTION**

  Use a RES instruction to reset a timer or counter.

  When the RES instruction is enabled, it resets the Timer On Delay (TON), Retentive Timer (RTO), Count Up (CTU), or Count Down (CTD) instruction having the same address as the RES instruction.

- **Cascading Timers**

  If an event requires a longer time-delay than a timer is capable of providing then multiple timers may be cascaded. That is, one timer completes a timing cycle and then activates another timer.



Counter Instructions Overview

- **Introduction**

  Counters are very essential in ladder logic programming. Counters are used to index, increment or decrement values.

Counter Instructions Parameters

The following parameters are associated with Counter instructions:

Each counter address is made of a 3-word element.

- **Word 1 is the control word**
  - Bit 0-7: Internal Use
  - Bit 10: UA - Update accumulation value.
  - Bit 11: UN - Underflow bit.
  - Bit 12: OV - Overflow bit.
  - Bit 13: DN - Done
  - Bit 14: CD - Count down is enabled.
  - Bit 15: CU - Count up is enabled.
- **Word 2 stores the preset value. (PRE)**
  - Specifies the value, which the counter must reach before the controller sets the done bit. When the accumulator value becomes equal to or greater than the preset value, the done status bit is set. You can use this bit to control an output device.
  - Preset value is from -32,768 to 32,767
- **Word 3 stores the accumulated value. (ACC)**
  - This is the number of times of false to true transitions that have occurred since the counter was last rest.

Counter Registers

Table 1.6 Counter Control Fields

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Word
CU	CD	DN	OV	UN	UA[1]				Internal Use[2]							0
Preset Value (PRE)																1
Accumulator Value (ACC)																2

(1) Fixed SLC 500 only.

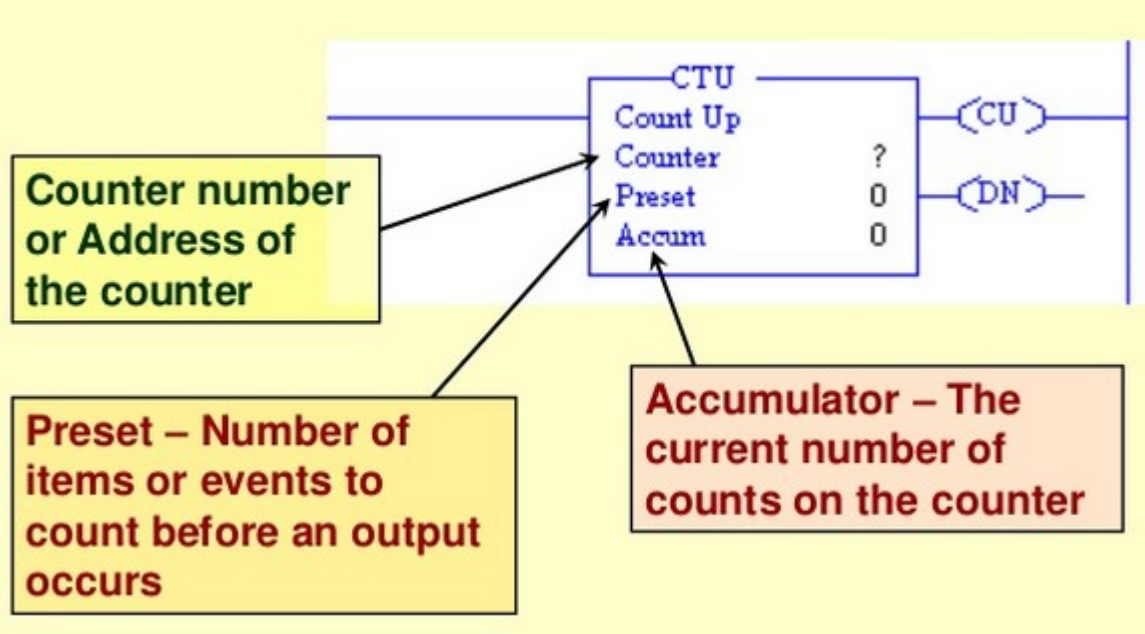
(2) Bits labeled "Internal Use" are not addressable.

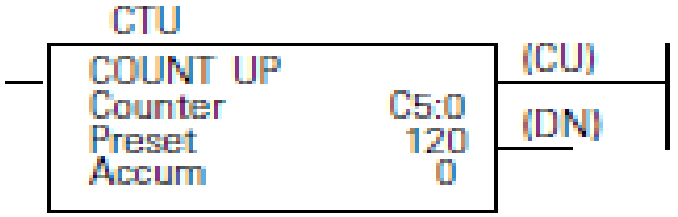
Addressable Bits	Addressable Words
CU = Count up enable (Bit 15)	PRE = Preset
CD = Count down enable (Bit 14)	ACC = Accum
DN = Done bit (Bit 13)	
OV = Overflow bit (Bit 12)	
UN = Underflow bit (Bit 11)	
UA = Update Accumulator bit (Bit 10) (Fixed Controller Only)	

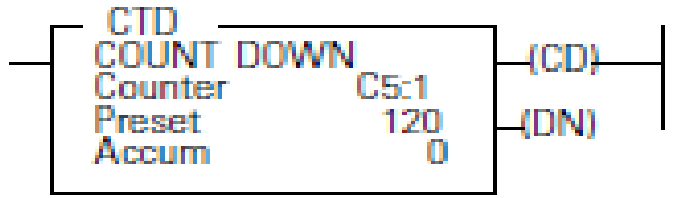
Counter Instructions

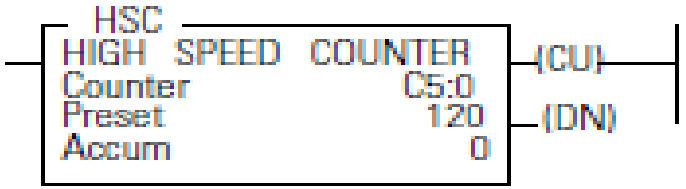
The following is a list of counter instructions in SLC 500:

- **CTU - Count Up**
- **CTD - Count Down**
- **HSC – High Speed Counter**



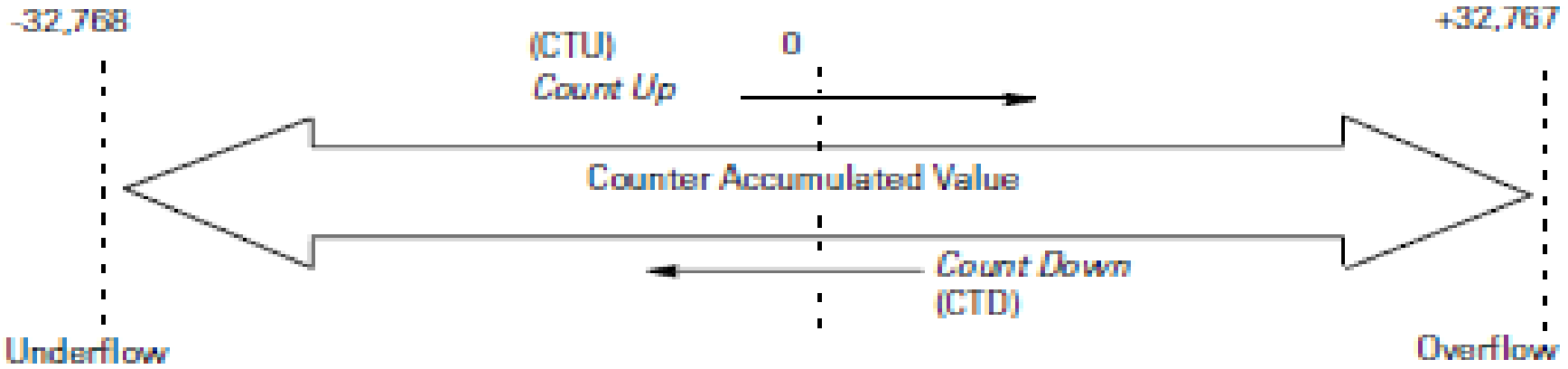






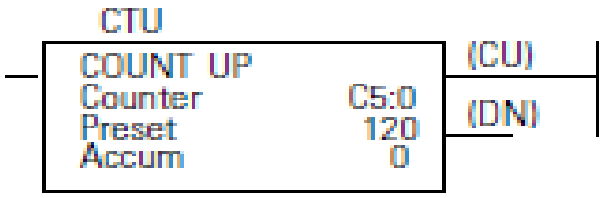
How Counters Work

- The figure below demonstrates how a counter works.
- The count value must remain in the range of -32768 to +32767. If the count value goes above +32767 or below -32768, the counter status overflow (OV) or underflow (UN) bit is set.
- A counter can be reset to zero using the reset (RES) instruction



CTU count up

Symbol

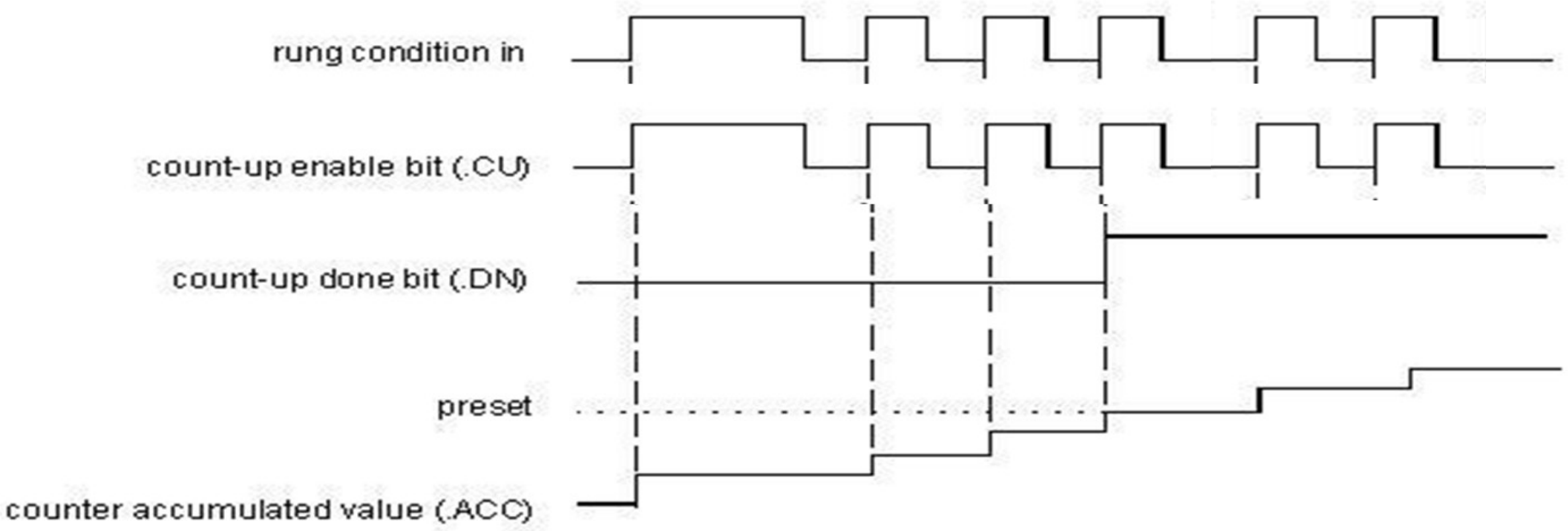


This Bit	Is Set When	And Remains Set Until One of the Following
Count Up Overflow Bit OV (Bit 12)	accumulated value wraps around to -32,768 (from +32,767) and continues counting up from there	a RES instruction having the same address as the CTU instruction is executed OR the count is decremented less than or equal to +32,767 with a CTD instruction
Done Bit DN (Bit 13)	accumulated value is equal to or greater than the preset value	the accumulated value becomes less than the preset value
Count Up Enable Bit CU (Bit 15)	rung conditions are true	rung conditions go false OR a RES instruction having the same address as the CTU instruction is enabled

Definition

- Increments the accumulated value at each false to true transition and retains the accumulated value when the instruction goes false or when power cycle occurs.
- The CTU is an instruction that counts false to true transition. When this transition happens the accumulated value is incremented by one count.
- A CTU accumulation is reset by the RES instruction.
- If the accumulation value is over the maximum range then the overflow (OV) bit will be true.

CTU Timing Diagram

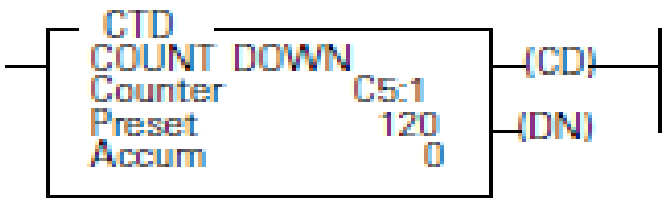


Example 4

- Count the number of times a photocell goes from off to on. Once we reach a count of 10 energize a light. We should also have a push button to reset the counter.
- **Input / Output**
  - Photocell I:1.0/0
  - Light O:2.0/0
  - Push Button I:1.0/1
- **Ladder Logic Solution**

CTD count down

Symbol

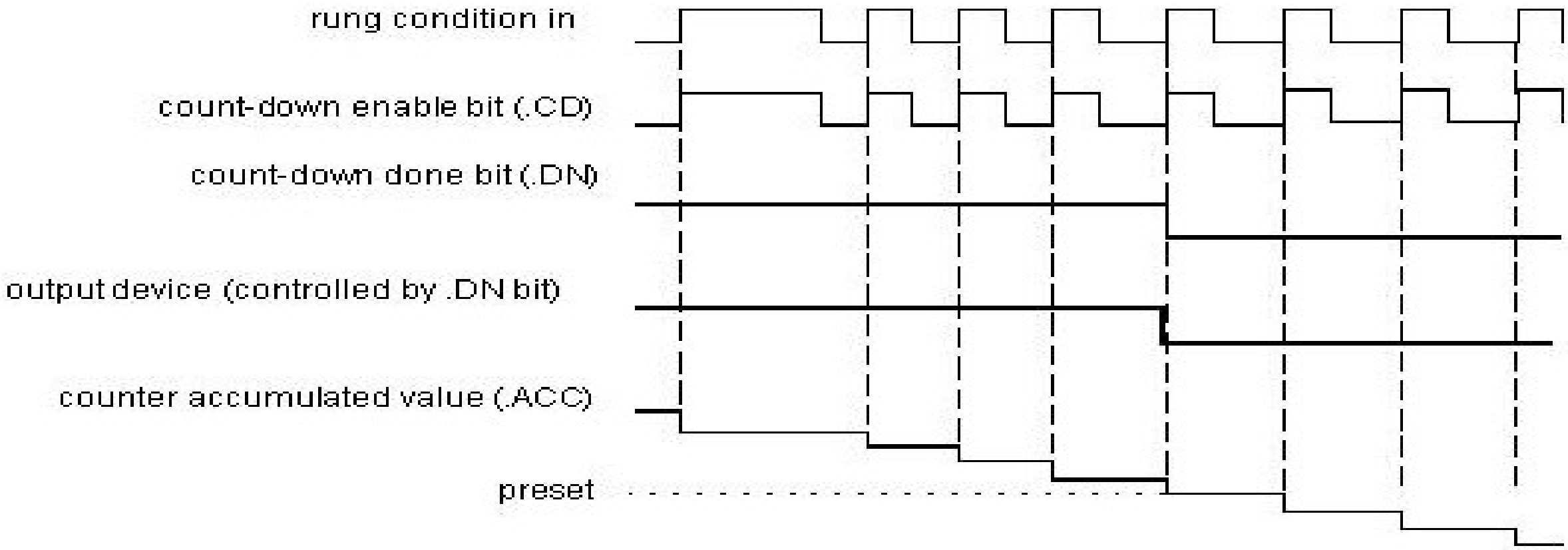


This Bit	Is Set When	And Remains Set Until One of the Following
Count Down Underflow Bit UN (Bit 11)	accumulated value wraps around to +32,767 (from -32,768) and continues counting down from there	a RES instruction having the same address as the CTD instruction is enabled. OR the count is incremented greater than or equal to +32,767 with a CTU instruction
Done Bit DN (Bit 13)	accumulated value is equal to or greater than the preset value	the accumulated value becomes less than the preset
Count Down Enable Bit CD (Bit 14)	rung conditions are true	rung conditions go false OR a RES instruction having the same address as the CTD instruction is enabled

Definition

- Decrements the accumulate value at each false to true transition and retains the accumulated value when the instruction goes false or when power cycle occurs.
- The CTD is an instruction that counts false to true transition. When this transition happen the accumulated value is decrements by one count.
- A CTD accumulation is reset by the RES instruction.
- If the accumulation value is below the minimum range then the underflow (UN) bit will be true.

CTD timing diagram



Example 5

- We want to have a count down on a proximity switch signal. Once we reach a count of 10 we will energize a light. When a push button is pressed then count will be reset.
- **Input / Output**
  - proximity switch I:1.0/0
  - Light O:2.0/0
  - Push Button I:1.0/1
- **Ladder Logic Solution**

Example 6

As a car enters the parking garage it triggers an up counter and increments the accumulator by one count.

As a car leaves the parking garage it triggers a down counter and decrements the accumulator by one count.

The up and down counters will use the same address. Since the counters have the same address the accumulated value is the same for both counters.

Whenever the accumulator value is equal to the preset value (50 car) the counter output is energized to light the “Lot Full” sign.

- **Input / Output**
  - Entrance gate Sensor I:1.0/0
  - Exit gate Sensor I:1.0/1
  - Lot Full Sign O:2.0/0
- **Ladder Logic Solution**

Programming Instructions