Electrical Circuits Lab. 0903219

Parallel RLC Resonance Circuit

- Parallel RLC Circuit Resonance Frequency *fr*:

* The definition of the resonance frequency ***fr*** is that it is the operating frequency that makes an **RLC** circuit a resistive circuit which means the imaginary part of the total impedance **Z** (or the total admittance **Y**) becomes zero.

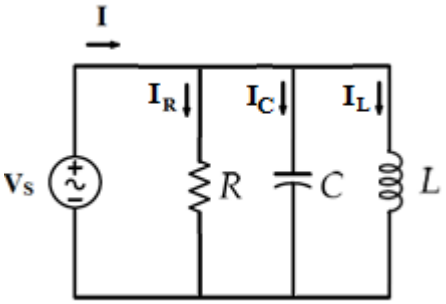


Figure (1) Parallel RLC circuit

* Depending on the above, we can find a formula for ***fr*** by following the steps shown below:

When $f = fr$ in a Parallel RLC circuit,

$$Im\{Y\} = 0$$

$$Im\left\{\frac{1}{R} + j\omega_r C + \frac{1}{j\omega_r L}\right\} = 0$$

$$j\omega_r C + \frac{1}{j\omega_r L} = 0$$

$$\rightarrow \quad j\omega_r C = \frac{-1}{j\omega_r L} \quad \rightarrow \quad \omega_r{}^2 = \frac{1}{LC}$$

$$\rightarrow \quad \omega_r = \frac{1}{\sqrt{LC}} \quad \rightarrow \quad fr = \frac{1}{2\pi\sqrt{LC}}.$$

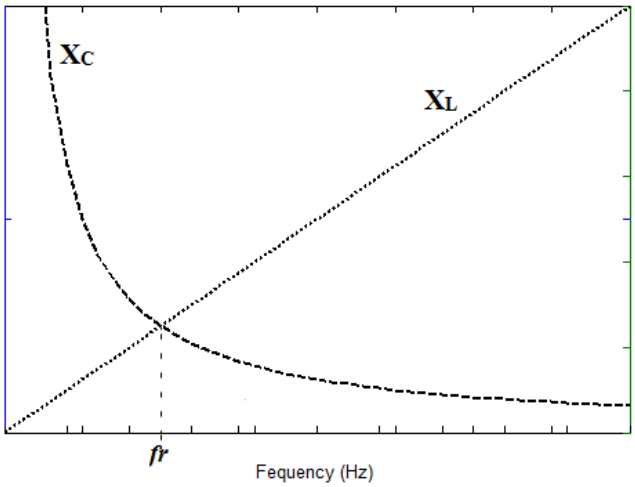


Figure (2) Frequency Response Curves for X_C and X_L reactance.

* Figure (2) shows important plot of how capacitor impedance X_C and inductor impedance X_L change with frequency and the place of ***fr*** on the plot (in this case when X_C equal X_L).

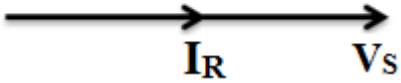
- Simple steps to draw phasor diagram of a parallel RLC circuit without memorizing! and important conclusions:

* Start with the quantity (voltage or current) that is common for resistor **R**, capacitor **C**, and inductor **L**, which is here the source voltage V_S (because it is parallel with all of them without being divided).

Step1

* Now, we know that $\mathbf{V_S}$ and resistor current $\mathbf{I_R}$ are in phase or have the same phase angle (also in time domain we see that there zero crossings are the same on the time axis) and $\mathbf{V_S}$ is greater than $\mathbf{I_R}$ in magnitude.

Step2



* Since $\mathbf{V_S}$ equal capacitor voltage $\mathbf{V_C}$ and equal inductor voltage $\mathbf{V_L}$, and we know that capacitor current $\mathbf{I_C}$ leads $\mathbf{V_C}$ by 90 degrees and inductor current $\mathbf{I_L}$ lags $\mathbf{V_L}$ by 90 degrees, both $\mathbf{I_L}$ and $\mathbf{I_C}$ will be on the imaginary axis, and the phasor diagram of a parallel RLC circuit will have three cases depending on the source operating frequency ***f*** :

a- Case 1: *f* = *fr*

As mentioned before when ***f* = *fr*** $\underline{\mathbf{X_L=X_C}}$ so $\underline{\mathbf{I_L=I_C}}$ and they are equal in magnitude and out of phase so $\mathbf{I_C}$ and $\mathbf{I_L}$ will cancel each other's effect and the circuit becomes a **resistive circuit** and the phase shift **Θ equal zero** (remember that $\Theta = \measuredangle \mathbf{I} = \measuredangle \mathbf{Y}$), the value of **current I is minimum and equals $\mathbf{V_S/R}$** and impedance **Z is maximum and equal R**.

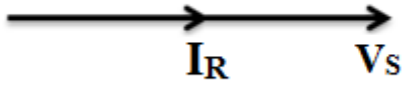


Figure (3) Parallel RLC Circuit Phasor Diagram when *f* = *fr*

b- Case 2: *f* < *fr*

Referring to Figure (2) notice that when ***f* < *fr*** $\underline{\mathbf{X_L<X_C}}$ so $\underline{\mathbf{I_L>I_C}}$ and the circuit becomes an **inductive circuit**, which means that **I lags $\mathbf{V_S}$ and Θ is a negative angle (with respect to $\mathbf{V_S}$)**.

From its phasor diagram in figure (4) we can conclude the following:

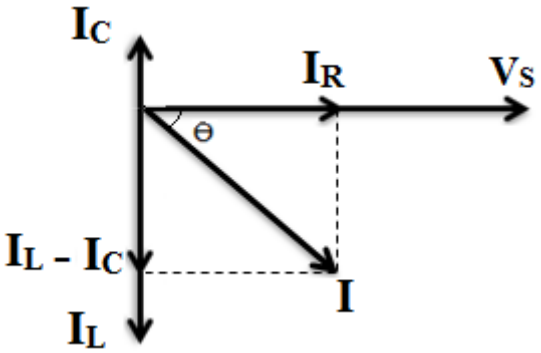


Figure (4) Parallel RLC Circuit Phasor Diagram when *f* < *fr*

1- $|\boldsymbol{V_S}| = \sqrt{(|\boldsymbol{I_L}| - |\boldsymbol{I_C}|)^2 + |\boldsymbol{I_R}|^2}$

2- $\Theta = \mathbf{tan^{-1}} \frac{|I_L|-|I_C| \ (\boldsymbol{imaginary\ part\ of\ I})}{I_R \ (\boldsymbol{real\ part\ of\ I})}$

and remember that $\Theta = \measuredangle \mathbf{I} = \measuredangle \mathbf{Y} = \mathbf{tan^{-1}} \frac{B_C-B_L \ (\textbf{imaginary part of Y})}{R \ (\textbf{real part of Y})}$

3- $|\mathbf{I_L}|$ and $|\mathbf{I_C}|$ can exceed the source current $|\mathbf{I}|$ but $|\mathbf{I_L}| - |\mathbf{I_C}|$ and $|\mathbf{I_R}|$ cannot.

c- Case 3: *f* > *fr*

Referring to Figure (2) notice that when ***f*** > ***fr*** $\underline{X_C < X_L}$ so $\underline{I_C > I_L}$ and the circuit becomes a **capacitive circuit**, which means that **I leads V_S and Θ is a positive angle (with respect to V_S)**.

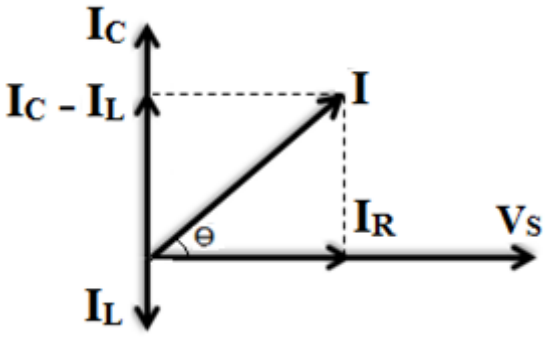


Figure (5) Parallel RLC Circuit Phasor Diagram when *f* >*fr*

From its phasor diagram in figure (5) we can conclude the following:

1- $|V_S| = \sqrt{(|I_C| - |I_L|)^2 + |I_R|^2}$

2- $\Theta = \tan^{-1} \frac{|I_C| - |I_L| \ (imaginary\ part\ of\ V_S)}{I_R \ (real\ part\ of\ V_S)}$

and remember that $\Theta = \measuredangle \mathbf{I} = \measuredangle \mathbf{Y} = \tan^{-1} \frac{B_L - B_C \ (\text{imaginary part of Z})}{R \ (\text{real part of Z})}$

3- $|\mathbf{I_C}|$ and $|\mathbf{I_L}|$ can exceed the source current $|\mathbf{I}|$ but $|\mathbf{I_C}| - |\mathbf{I_L}|$ and $|\mathbf{I_R}|$ cannot.

- How the circuit quantities change with frequency:

* Figure (2) and the circuit phasor diagram helps in finding the circuit quantities change with voltage source frequency ***f*** changing.

* As shown in figure (2), at low frequency ***f*** the difference between $\mathbf{X_C}$ and $\mathbf{X_L}$ is huge but with ***f*** increasing this difference starts to decrease so **Z** will increase until ***f*** reaches ***fr*** where **Z** becomes maximum, after ***f*** exceeds ***fr***, the difference between $\mathbf{X_C}$ and $\mathbf{X_L}$ incraeses with frequency incraesing so **Z** will decrease. In a concise way, the total impedance **Z** will increase before ***f*** reach ***fr*** then decrease when ***f*** exceeds ***fr*** and it's value is maximum at resonance frequency and equals **R** as shown in figure (6).

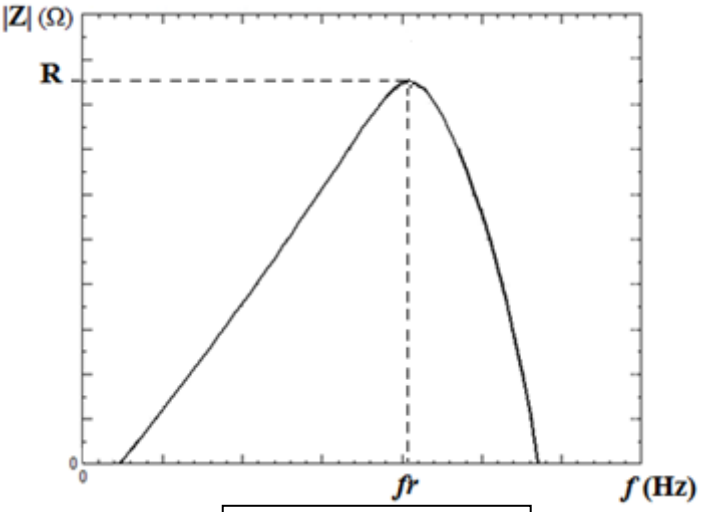


Figure (6) |Z| vs. *f*

* **Θ** ranges from -90° to 90° (-90° < **Θ** < 90°). And since $|\Theta| = \tan^{-1} \frac{|B_C - B_L|}{R}$ and the $\tan^{-1}$ function is increasing on the interval from -90° to 90°, the phase shift **Θ** (or the current angle $\measuredangle \mathbf{I}$) will decrease before ***f*** reach ***fr*** then increase when ***f*** exceeds ***fr*** and it's value is minimum at resonance frequency and equals **zero** as shown in figure (7).

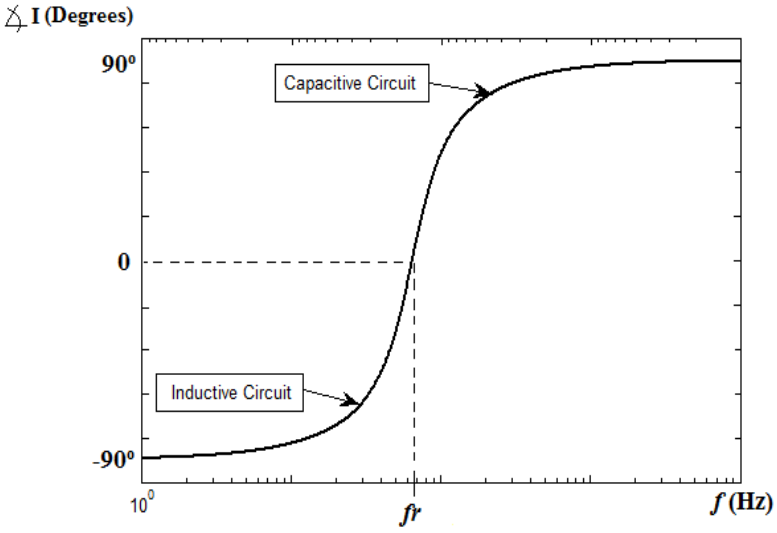


Figure (7) Θ vs. *f*

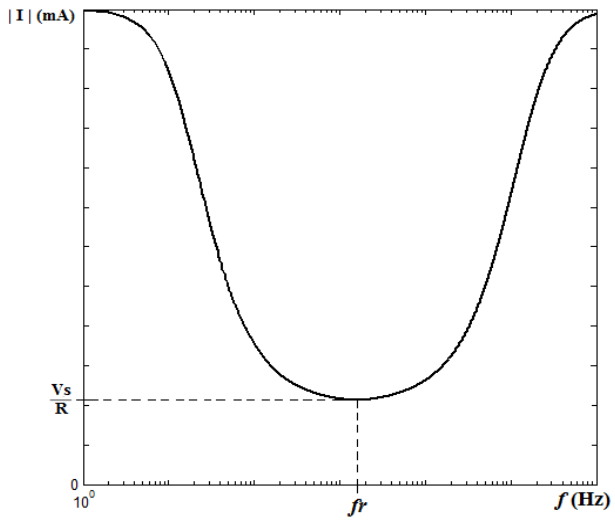


Figure (8) | I | vs. *f*

* Because **I** is inversely proportional to **Z**, the total current **I** will decrease before ***f*** reaches ***fr*** then increase when ***f*** exceeds ***fr*** and it's value is minimum at resonance frequency ***fr*** and equals $\mathbf{V_S/R}$ as shown in figure (8).

* Figure (9) shows $\mathbf{I_R}$,$\mathbf{I_L}$ and $\mathbf{I_C}$ frequency response curves.

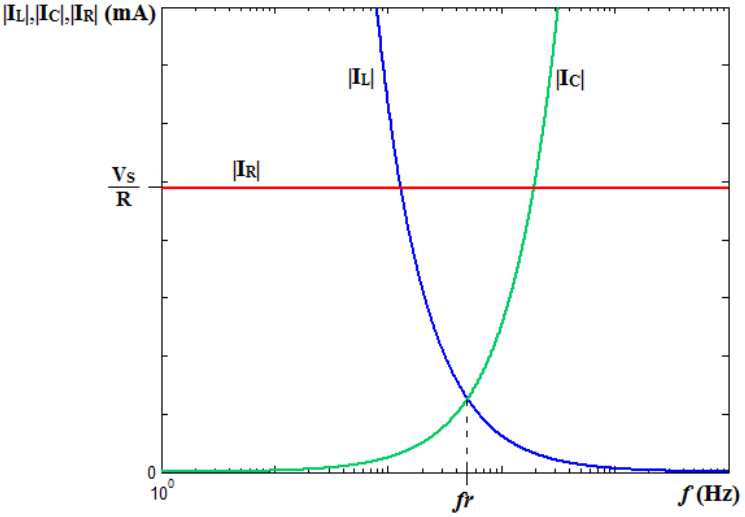


Figure (9) $|\mathbf{I_R}|$,$|\mathbf{I_L}|$ and $|\mathbf{I_C}|$ vs. *f*

- Figure (10) below shows a time domain representation for all the vectors shown on the phasor diagram for the case *f* < *fr*:

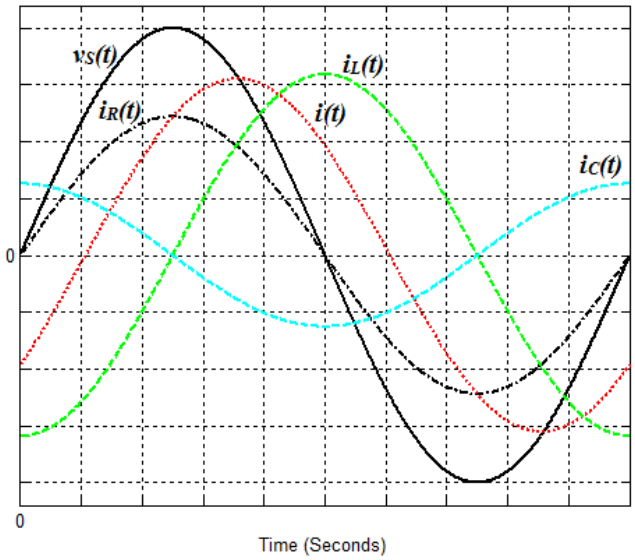


Figure (10) Parallel RLC Circuit Time Domain Representation

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